2. 3. (Amended) A method as claimed in Claim 1 wherein an electroplating waveform is used, at least in part, to ensure the sufficiently small copper grain size generation within the recessed microstructures.

3. 4. (Amended) A method as claimed in Claim 1 wherein an electroplating solution additive is used, at least in part, to ensure the sufficiently small copper grain size generation within the recessed microstructures.

4. 6. (Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

depositing copper into the recessed microstructures using an electrochemical process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures; and

subjecting the surface of the semiconductor workpiece and the deposited copper to an elevated temperature annealing process at a temperature at or below about 250 degrees Celsius for a time period that is sufficient to increase the grain size of the deposited copper.

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5. 8. (Amended) A method as claimed in Claim 4 wherein an electroplating waveform is used, at least in part, to ensure the sufficiently small metal grain size.

6. 9. (Amended) A method as claimed in Claim 4 wherein an electroplating solution additive is used, at least in part, to ensure the sufficiently small metal grain size.

1. 10. (Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece, the workpiece including at least one low-K dielectric layer, with copper metal comprising:

depositing copper into the recessed micro-structures using an electrochemical process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures; and

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subjecting the surface of the semiconductor workpiece with the deposited copper to an elevated temperature annealing process at a temperature selected to be below a predetermined temperature at which the low-K dielectric layer would suffer substantial degradation.

8. (Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one low-K dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one dielectric layer;

preparing a surface of the workpiece including the recessed microstructures with a metal seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer onto the surface of the workpiece using a process that generates copper grains that are sufficiently small to substantially fill the recessed microstructures;

annealing the electrochemically deposited copper layer at an elevated temperature selected to be below a predetermined temperature at which time the low-K dielectric layer would substantially degrade for a predetermined period of time; and

removing copper metallization from the surface of the workpiece except from the recessed microstructures, after the annealing of the copper.

9. A method as claimed in Claim 8 wherein the predetermined period is greater than about 20 hours.

10. (Amended) A method as claimed in Claim 8 wherein the step of preparing a surface of the workpiece comprises:

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applying at least one barrier layer over the dielectric layer; and

applying a metal seed layer over the barrier layer.

11. 14. A method as claimed in Claim 10 13 wherein the step of applying the seed layer is defined by applying the seed layer using a chemical vapor deposition process.

12. 15. A method as claimed in Claim 10 13 wherein the step of applying the seed layer is defined by applying the seed layer using a physical vapor deposition process.

13. 16. (Amended) A method as claimed in Claim 8 11 wherein the step of preparing a surface of the workpiece comprises:

applying at least one adhesion layer over the dielectric layer; and

applying a metal seed layer over the adhesion layer.

14. 17. A method as claimed in Claim 8 11 wherein the step of removing the copper metallization is defined by removing the copper metallization using a chemical mechanical polish technique.

15. 24. (Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one dielectric layer;

preparing a surface of the workpiece, including the recessed microstructures, with a seed layer for subsequent electrochemical copper deposition;

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electrochemically depositing a copper layer onto the surface of the workpiece using a process generating copper grains that are sufficiently small to substantially fill the recessed microstructures; and

subjecting the electrochemically deposited copper layer to an annealing process at a temperature at or below about 250 to 300 degrees Celsius to increase the copper grain size.

16. ~~25~~. A method as claimed in Claim ~~24~~ 15 wherein the step of preparing a surface of the workpiece comprises:

applying at least one adhesion layer over the dielectric layer; and

applying a seed layer over the adhesion layer.

17. ~~26~~. A method as claimed in Claim ~~24~~ 15 wherein the step of preparing a surface of the workpiece comprises:

applying at least one barrier layer over the dielectric layer; and

applying a seed layer over the barrier layer.

18. ~~27~~. A method as claimed in Claim ~~26~~ 17 wherein the step of applying the seed layer is defined by applying the seed layer using a chemical vapor deposition process.

19. ~~28~~. A method as claimed in Claim ~~26~~ 17 wherein the step of applying the seed layer is defined by applying the seed layer using a physical vapor deposition process.

20. ~~29~~. A method as claimed in Claim ~~24~~ 15 wherein the step of removing the copper metallization is defined by removing the copper metallization using a chemical mechanical polish technique.

21. ~~30~~. (Amended) A method for filling recessed microstructures at a surface of a semiconductor workpiece with copper metal comprising:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

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applying at least one low-K dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed microstructures in the at least one low-K dielectric layer;

preparing a surface of the workpiece, including the recessed microstructures, with a barrier layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer to the surface of the workpiece using a process that generates copper grains having a size sufficiently small to substantially fill the recessed microstructures; and

subjecting the electrochemically deposited copper layer to an annealing process at a temperature below which the low-K dielectric layer substantially degrades.

~~21~~ 22. A method as claimed in Claim ~~20~~ 21 wherein the annealing step takes place at a temperature corresponding to a baking temperature of the low-K dielectric.

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1420 Fifth Avenue
Suite 2800
Seattle, Washington 98101
206.682.8100